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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
MONDT, JOHANNES P	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/633,993
Filing Date: August 04, 2003
Appellant(s): HYNECEK, JAROSLAV

Alan K. Stewart (Reg. No.: 35,373) (Texas Instruments, Incorporated, Patent Department, Dallas, Texas 75265)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 2/20/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Status of the Claims

The statement of the status of claims contained in the brief is correct.

(3) Status of Amendments

The status of the amendments is as stated in the appeal brief, however only the amendment under 37 C.F.R. 1.111 on May 11, 2005 has been entered while the

amendment under 37 C.F.R. 1.116 submitted on November 18, 2005 was filed on November 29, 2005 and has *not* been entered; the latter only consists of Remarks; in particular, the claim language to date is that of the amendment under 37 C.F.R. 1.111 on May 11, 2005.

(4) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(5) Grounds of rejection to be reviewed upon appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(6) The claims appendix

The claims appendix representing all pending elected claims is correct.

(7) Evidence Appendix

Here Appellant states "None".

(8) Related Proceedings Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(9)-a Prior Art of Record and applied in the Final Action to appealed rejection of claim 11

5,502,318	HYNECEK	03-1996
5,388,137	BOSIERS ET AL.	02-1995
5,760,430	KATO	06-1998

(9)-b Other Prior Art of Record

4,173,064	Farnow, Stephen A.	11/1979
4,857,979	McNutt, Michael J.	08-1989
6,278,142 B1	Hynecek, Jaroslav	08-2001
5,430,481	Hynecek, Jaroslav	07-1995
4,229,752	Hynecek, Jaroslav	10-1980
5,337,340	Hynecek, Jaroslav	08-1994
5,442,395	Hynecek, Jaroslav	08-1995

(10) The Final Rejection

Only for convenience to the reader the Final Rejection contained in the Office Action mailed 9/20/06 is herewith being reproduced, but without any change intended.

BEGIN FINAL REJECTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by Hynecek (5,502,318). Hynecek teaches a charge coupled device comprising: a first clocked gate 24/28 coupled to a first clocking signal $\phi 1$ (Figure 1 and col. 2, l. 43-55 and col. 3, l. 1-17); a field plate 40/42/44/46 adjacent to and surrounding the first clocked gate (col. 2, l.

56-67 and col. 3, l. 1-17), and coupled to a DC bias source V_{bias} (col. 3, l. 1-17); and a second clocked gate 26 adjacent to an surrounded by the field plate and coupled to a second clocking signal f2 (col. 2, l. 43-55 and col. 3, l. 1-17), the field plate separates the first clocked gate from the second clocked gate (Figure 1), and the first clocking signal is clocked out of phase with the second clocking signal (col. 3, l. 8-10). In conclusion, claim 11 is anticipated by Hynecek.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bosiers et al (5,388,137) in view of Kato (5,760,430) (previously made of record).

Bosiers et al teach (title, abstract, cols. 4-8 and Figure 4) a charge coupled device comprising:

a first clocked gate 39 (col. 6, l. 11) coupled to a first clocking signal ϕ_2(col. 6, l. 50-56):

a field plate 38 (col. 6, l. 11) adjacent to and surrounding the first clocked gate (Figure 4); and

a second clocked gate 41 (col. 6, l. 11) adjacent to and surrounded by the field plate (Figure 4) and coupled to a second clocking signal ϕ_4 (col. 6, l. 50-55), the field

plate is between the first clocked gate 39 and the second clocked gate 41 (Figure 4), and the first clocking signal is clocked out of phase with the second clocking signal (Figure 5).

Bosiers et al do not necessarily teach the limitation that said field plate to be coupled to a DC bias source.

However, it would have been obvious to include said limitation in view o Kato, who teach the possibility to reduce the number of required clocks (cf. abstract) by coupling the equivalent 14 of field plate 38 to a DC signal source 18 (see Figure 1 and col. 6, l. 7-24). *Motivation* to include the teaching by Kato in the invention by Bosiers et al derives from the resulting decrease in complexity of the clock system through reduction of the number of clocks required.

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bosiers et al and Kato as applied to claim 11 and further in view of McNutt (4,857,979) (previously made of record). As detailed above, claim 11 is unpatentable over Bosiers et al in view of Kato. Bosiers et al also teach a well region 33 (cf. col. 6, l. 4), but *do not necessarily* teach well regions under clocked gates, nor a clocked barrier. *However, it would have been obvious* to include said clocked barrier and clocked well in view of McNutt, who, in a patent on an infrared CCD imaging device (title, abstract, col. 1, col. 2, l. 1- col. 2, l. 27 and col. 2, l. 53 – col. 4, l. 50), hence closely related to the invention by Bosiers et al, teaches the inclusion of a clocked well 58 (cf. col. 4, l. 21) and barrier gate 52 (cf. col. 4, l. 22) to a clocked gate so as to prevent back-flow of charge carriers (cf. col. 4, l. 21-28). *Motivation* to include the teaching by McNutt into the

invention by Bosiers et al derives from the enhanced control on the motion of collected charges. The teaching can be combined readily by adding the barrier gate and doping the substrate to each clocked gate.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bosiers et al and Kato as applied to claim 11, and further in view of Hynecek (5,430,481) (IDS item AC). As detailed above, claim 11 is unpatentable over Bosiers et al in view of Kato. Bosiers et al nor Kato necessarily teach the further limitation as defined by claim 14, although Bosiers et al do disclose a solid-state imaging apparatus using their CCD device (cf. col. 4, l. 6-12). *However, it would have been obvious to include* said further limitation in view of *Hynecek*, who, in a patent on a CCD image sensor, - hence analogous art, teaches the incorporation of a charge transfer device into a solid-state imaging apparatus of the frame transfer type (cf. abstract). In particular, Hynecek teaches the incorporation of the CCD device in an imager including a frame transfer image array defined by reference to this patent in Applicant's specification and as depicted in Figure 1 and described in col. 2, l. 25-48), with the following attributes: two phase imaging area 22, single phase frame memory area 24, dual serial registers 26 and 28, charge detection amplifiers 30 and 32, bottom clearing drain 34, and external connections 12. *Motivation* for inclusion of the teaching by Hynecek in the invention by Bosiers et al and Kato is the obviously advantageous application of the CCD device component to an imager compatible with both the NTSC standard and requirements for still photography (col. 1, l. 15-35). *Combination* of the teaching in this regard by

Hynecek in the invention by Bosiers et al is easily accomplished by replacement of the component for moving the charges.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hynecek (5,502,318) in view of Hynecek (6,278,142 B1), henceforth called "Hynecek_2", previously made of record. As detailed above, Hynecek (5,502,318) anticipates claim 11. Hynecek does not necessarily teach a full frame device, but does indicate a full frame device can be built using the CCD device taught by Hynecek (col. 6, l. 24-49). It would have been obvious to follow through on this suggestion by Hynecek in view of Hynecek_2, teaching inter alia an IMPACTRON cell (Figures 5-6), which is the defining portion of a Full Frame device (col. 7, l. 56-64 in Hynecek_2). *Motivation* derives from the obviousness to apply the invention to an area of application already indicated by the inventor.

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hynecek (5,502,318) in view of Farnow (4,173,064). As detailed above, Hynecek anticipates claim 11. Hynecek does not necessarily teach an anti-blooming drain. However, it would have been obvious to include an anti-blooming drain in view of Farnow, who teaches an anti-blooming drain for the removal of excess signal charge generated in response to optical overload of a CCD sensing region (abstract and col. 4, l. 19-44). Motivation to include the teaching by Farnow in the device by Hynecek derives from the removal of "blooming", i.e., the spreading of charge from a light sensing element illuminated much more brightly than adjacent light sensing elements to said adjacent light sensing elements, causing a blur in the image (col. 1, l. 37-56 in Farnow).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bosiers et al and Kato as applied to claim 11 above, and further in view of Hynecek (5,337,340) (IDS item AB). As detailed above, claim 11 is unpatentable over Bosiers et al in view of Kato. Neither Bosiers et al nor Kato necessarily teach the further limitation that the device is a charge-multiplying device. However, it would have been obvious to include said further limitation in view of Hynecek (5,337,340) (IDS item AB), who teaches a CCD device that is a charge multiplying device through appropriate selection of the voltage difference between subsequent clocked gates (ϕ_3 and ϕ_4), causing charge multiplication through impact ionization (cols. 1-3 and cols. 4-5, in particular col. 5, lines 30-49). *Motivation* to include the teaching by Hynecek in the device by Bosiers et al derives from the teaching by Hynecek of increased sensitivity through charge-multiplication (col. 1, l. 25-col. 2, l. 41).

END OF FINAL REJECTION

(11) Examiner's Answer to Argument

The following answer from the examiner is offered in response to the argument in the appeal brief. As evidenced overleaf Appellant both rejections of claim 11 as reproduced above.

(A) Rejection under 35 USC 102(b) as being anticipated by US Patent 5,502,318 to Hynecek.:

Argument by Appellant is exclusively based on the allegation that regions 40, 42, 44 and 46 "are bipolar gates but not field plates" (see page 6 of Appeal Brief). This argument is not persuasive for the following reasons:

The Specification by Appellant does not specifically define "field plate". Well-known dictionaries such as McGraw-Hill Dictionary of Scientific and Technical Terms" (Sixth Edition (2003)), the "Comprehensive Dictionary of Electrical Engineering" (CRC Press, CRC Handbook Published in Cooperation with IEEE Press, 1999), and the "The Authoritative Dictionary of IEEE Standards Terms", seventh edition, do not define "field plate".

The "field plate" by Appellant is first introduced in the elected invention through Figure 3 (see page 11), which is a cross-sectional illustration of the elected invention, showing as "field plate gate" that can be described as a conductive region (region 305) capable of influencing the voltage in a nearby portion of the wafer by being connected to a bias voltage, for which reasons the examiner has assumed the above underscored portion to be a substitute definition of "field plate". Both region 305 of the specification and the region 40/42/44/46 in the reference meet this definition and both are poly-silicon regions; they both are connected to a DC bias voltage (loc.cit.), are thus both non-clocked. See page 4 for the first occurrence of "field plates" in the specification, particularly in the "Brief Description of the Drawings", and see page 10, line 23 for its first occurrence in the "Detailed Description of Preferred Embodiments".

This definition is substantially supported by the use of the term "field plate" in the semiconductor device art. See, for instance, (a) Kimura et al (EP 0 216 380 A2)

(published in 1986) disclosing a "field plate electrode" 15 capable of influencing the voltage in a nearby portion of the wafer, being connected to a bias voltage (see column 1 and Figure 2), and see also (b) Tihanyi (USPAT 6,362,505 B1) (published 2002) disclosing as prior art a "field plate" 4 in a wafer capable of influencing the voltage in nearby wafer portion 3 (drift zone) (see Figure 4 and col. 1, l. 49-63). Both examples confirm the above definition. Furthermore, example (a) demonstrates that a field plate may well abut the nearby region in the wafer, while example (b) demonstrates that a field plate may well be located within the wafer.

It follows directly that the argument that said reference "does not disclose the field plate" (page 6, final paragraph, of Appeal Brief) is not correct: specifically, structure 40/42/44/46 of the reference forms a region of the same material constitution (polysilicon) as inventor's structure 305, and like the latter, is kept at a single DC bias voltage, thus influencing, in fact substantially determining, the voltage at a nearby portion of the wafer, just as structure 305 does influence, in fact substantially determine, the voltage at a nearby portion of the wafer.

The amplification of said argument by Appellant that regions 40/42/44/46 are instead "bipolar gates" is irrelevant at least because they are a "field plate" as discussed above, while Appellant, in his specification, has not distinguished his "field plates" from "bipolar gates". "Bipolar gates" are not mentioned in the specification for any purpose, be it for distinction or otherwise.

Examiner concludes in light of the above considerations that the "field plate" as claimed does not patentably distinguish over the structure 40/42/44/46 of the prior art as cited and that the rejection over this reference should be maintained.

(B) Rejection under 35 USC 103(a) as being unpatentable over US Patent 5,388,137 to Bosiers et al in view of US Patent 5,760,430 to Kato.

Argument by Appellant is based on two points of traverse differing only in slight alteration of language, namely:

(1) on the allegation that "gate 38 in US Patent 5,388,137 does not surround the first clocked gate 39", and that, therefore, "there is no field plate adjacent to and surrounding the first clocked gate" (see page 7 of the Appeal Brief). This is not persuasive for the following reasons: "surrounded" is first introduced in the specification of Appellant in cross-sectional Figure 3 where first clocked gate, i.e., gate structure 309, is said to be "surrounded" by field plate 305. In the same cross-sectional context, in the first reference (US Patent 5,388,137) the field plate 38 surrounds the first clocked gate structure 39 and the second clocked gate 41 is surrounded by the field plate 38. Nowhere in the specification is "surrounded" defined either explicitly, let alone more narrowly. In both specification of Appellant and reference (US Patent 5,388,137) the field plate is at least seen to "extend around an edge or margin of the first clocked gate" and within the context of a cross-sectional rendition the field plate is in both the

specification and the reference seen to "enclose on all sides" the first clocked gate. Therefore, the use of "surround" with regard to Figure 3 in the specification, where "surround" is first introduced with regard to the relation between the field plate and the first clocked gate is fully compatible with at least two meanings in common language of the verb "surround" as listed in Merriam-Webster's Collegiate Dictionary of the English language, 10th Edition (1998), page 1187, particularly meanings a and d, i.e., a: to "enclose on all sides" (which is true in the context where "surround" is first introduced, namely: the cross-sectional illustration given by Figure 3), and d: "to extend around the margin or edge". To "surround", in the examiner's broadest possible interpretation when applied in light of the specification neither necessarily implies "encircle"; nor does "surround" in said broadest possible interpretation necessarily implies "abut". Furthermore, although Appellant does not specifically argues on the basis of an alleged failure to show the limitations "adjacent", examiner makes of record herewith that according to the same dictionary "adjacent" means, inter alia, "nearby" (see Merriam-Webster-s Collegiate Dictionary, 10th Edition, (1998), page 14; hence field plate 38 is adjacent to and surrounds first clocked gate 39; similarly, second clocked gate 41 is "adjacent to and surrounded" by field plate 38, thus meeting the claim language. In both cases only an insulating layer separates clocked gate and field plate, which is an inherent requirement for the independent functioning of field plate and clocked gate.

(2) for the same reason the final argument by Appellant that gate 40 "is on the other side of clocked gate 39" (final sentence of Argument on page 7 of Appeal Brief)

does not invalidate the conclusion from Figure 4 in US Patent 5,388,137 that field plate 38 is "adjacent to" (on the left side of 39 with minimal separation given the required independent functionalities of cloaked gates and field plate) and "surrounds" (i.e., "encloses on all sides" (meaning "a" in Merriam-Webster (loc.cit.) (i.e., all sides shown in Figure 3 where "surround" is introduced) and "extends around the margin or edge" (meaning "d" in Merriam-Webster, loc.cit.) of the first clocked gate.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 3600

JPM
April 11, 2006
Conferees
Drew A. Dunn, Nathan Flynn, Johannes Mondt

TEXAS INSTRUMENTS, INCORPORATED
P. O. BOX 655474-M/S 3999
PATENT DEPARTMENT
DALLAS, TEXAS 75265
972/917-5466